SECTION 17
YA BOARD

17-1. CPU SYSTEM

The CPU of this unit is a 32-bit RISC microprocessor. All control operations of the unit are performed by one chip. The circuits of the YA board can broadly be divided into four blocks.

- CPU
  - MAIN BLOCK
    - SIRCS processing
    - +5 V supply to commander
    - Set protector
    - 7 seg. LED control
  - COMM. BLOCK
    - RS-232C communication
    - RS-422A communication
    - RS-485 communication
  - REGI BLOCK
    - I^2C control
    - Regi DAC control
    - G2 control
    - Sync separate
    - Frequency detect
    - Data save/load
  - OSD BLOCK
    - OSD processing
    - Character and internal signal generation
    - V-shift control
    - Blanking control

17-1-1. Main Devices of YA Board

CPU	HD6437043AF28	
Address dec.	UPD65646GJ-252-8EU	Sub µcom•SIRCS control
Sub µcom	CXP846P48Q	SIRCS encoder/decoder
UV-EPROM	M27C4002-10F1	Uploader
Program Flash ROM	MBM29F800BA-70PFTN	Main program
S-RAM	IDT71024S15Y∗2	
I/O Port ④	UPD65646GJ-252-8EU	Set protector
7 seg. LED driver	EPM7128STC100-15-DRV	7 seg. LED control
Serial I/F with FIFO	PC16552DV	Serial communication
RS-232C driver	MAX202ECSE	RS-232C control
RS-485 driver	MAX3085CSA∗2	RS-485 control
RS-422A driver	MAX489ECSD	RS-422A control
I/O Port ②	UPD65646GJ-252-8EU	IFB control, I^2C control, various differentiation operations
Battery S-RAM	DS1245Y-120	User data save (Expandable to 512 kbytes)
Backup Flash ROM	MBM29F040C-90PD	Service/Factory data save
Regi DAC controller	CXD305-127R	DAC control for registration
G2 DAC controller	CXD2309Q	DAC control for G2
Freq. Det. G/A	UPD65654GC-327-3B6	Freq. Det.
Sync sep. G/A	CXD8773R	Sync control
ODS G/A	UPD65806GD-064	OSD control
S-RAM	IDT71016S15Y∗2	
I/O Port ③	UPD65646GJ-252-8EU	OSDC control, PLL control
Clock driver	MC10H640FN	2CLK driver
CMD Dualport RAM	IDT71321S55J	OSD command RAM
FONT Flash ROM	MBM29F400BC-70PFTN	OSD FONT DATA

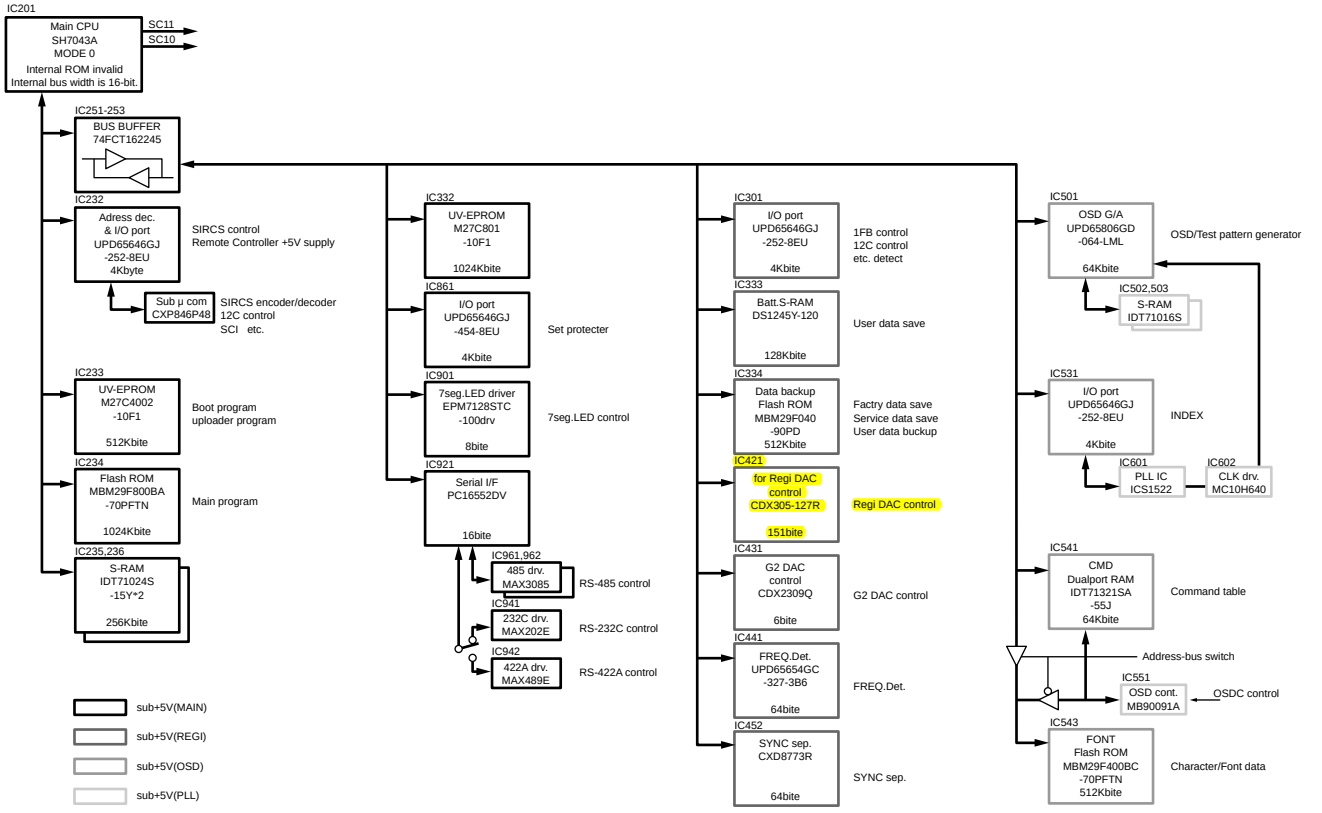

Fig. 17-1

17-4. I²C CONTROL

The I²C bus performs serial communication with the I²C device using two lines SCL and SDA.

As no control is performed during set standby, the line connected to this line is separated by incorporating a bus switch to prevent current leakage during standby.
The I²C bus mainly performs control of the small signal circuit on the BA board.

17-5. DAC CONTROL

17-5-1. Registration DAC Control

The DAC IC control for adjusting registration on the D board is performed by eight control lines-D-SCL, D-SDA0, D-SDA1, D-SDA2, D-LD0, D-LD1, D-LD2, and D-LD3.
To control one channel DAC, 12-bit DAC data (including the DAC address), CLK for data shift, and LD pulse for inputting the data are required. The actual IC incorporates a 8-ch DAC.

DAC control waveform (For one channel)

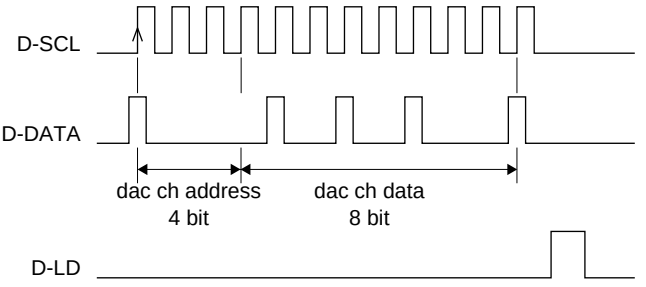

Fig. 17-6

This DAC IC also has a SDO terminal (Serial Data Out). As it can be cascade connected, a group of DAC ICs can be formed by cascade connection so that several DACs can be controlled at one time.
In the D board, six of these DAC ICs are cascade connected to form one group and there are altogether twelve groups.
In order to control all DACs, 12-bit × 6 × 8-channel 12-group data is required.

One group

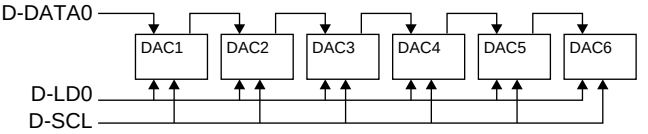

Fig. 17-7

DAC control waveform (1 group)

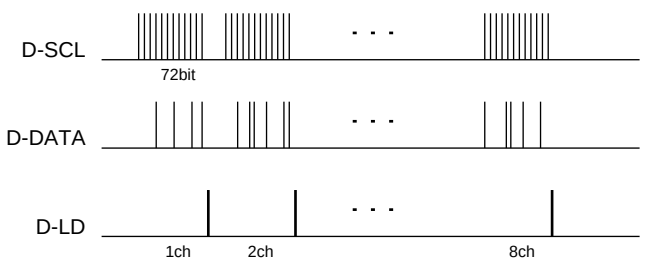

Fig. 17-8

Taking into consideration effects on the images, data is transferred to the DAC within about half (180 us) the VD period (flyback period) taking the deflection return VD as the trigger.
The transfer CLK is about 5 MHz.
In the YA board, data of three groups are temporarily stored in IC421 during the video period, and data transfer is started at the same time the VD period starts.
Consequently, 4VD is required to control the DAC of all twelve groups.

17-6. SYNC PROCESSING

17-6-1. Sync Sep. G/A (IC452)

A newly developed IC which performs input sync presence detection, input sync polarity detection, output sync polarity standardization, H/V separation, H-sync width standardization, clamp pulse generation, interlace differentiation, and frequency detection.

Input sync presence detection

H/C sync : For the RGB input, the signal connected to the H/C-sync input terminal on the BA board is input.
For the video input, the sync-separated composite-sync by the BA board is input.
- Determined as present when SYNC is input in the 16H continuous period.
- Determined as absent when SYNC is not input even one time for 6.2 msec. in the continuous period.

V sync : For the RGB input, the signal connected to the V-sync input terminal on the BA board is input.
For the video input, the sync-separated V-sync is input by the BA board.
- Determined as present when V SYNC is input even once in the 8192H period.
- Determined as absent when V SYNC is not input even once in the 8192H period.

SonG : Green is input for the RGB input and the signal sync-separated by the BA board is input for the video input.

Input sync polarity detection, standardization output

As the polarity of the H/V sync input to the YA board is not standardized by the type of input signal, the polarity is determined inside G/A, and at the same time, the negative polarity is standardized and output.

H/V Separation

When the sync source selected is C-sync, SonG, the signal is separated into H-sync and V-sync, and output to the deflection block. This is then performed without adjustments to 15 to 150 kHz by the digital H/V separator in the G/A block. If the equivalent pulse is present, it is extracted and output.